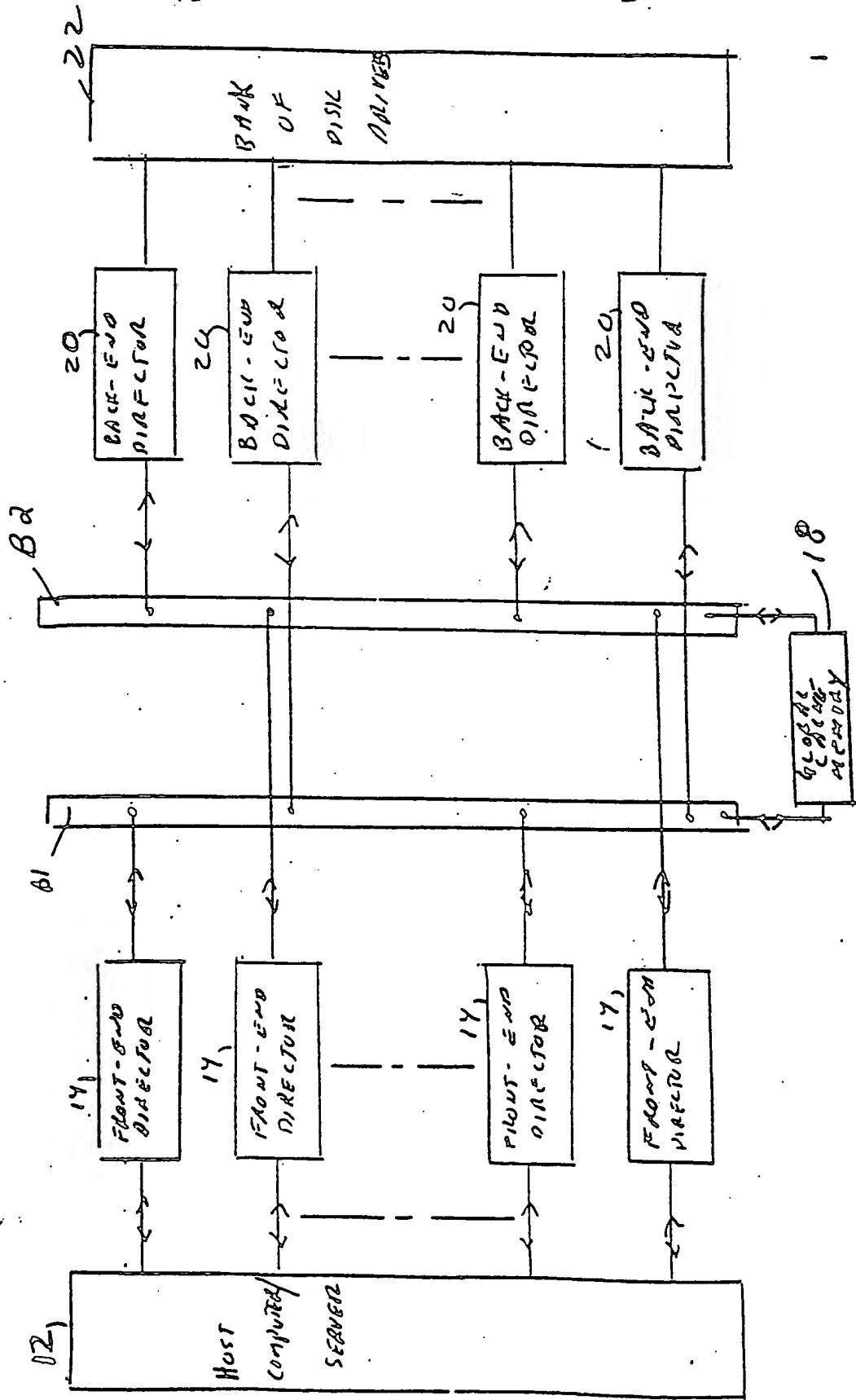


FIG. 1
Data net



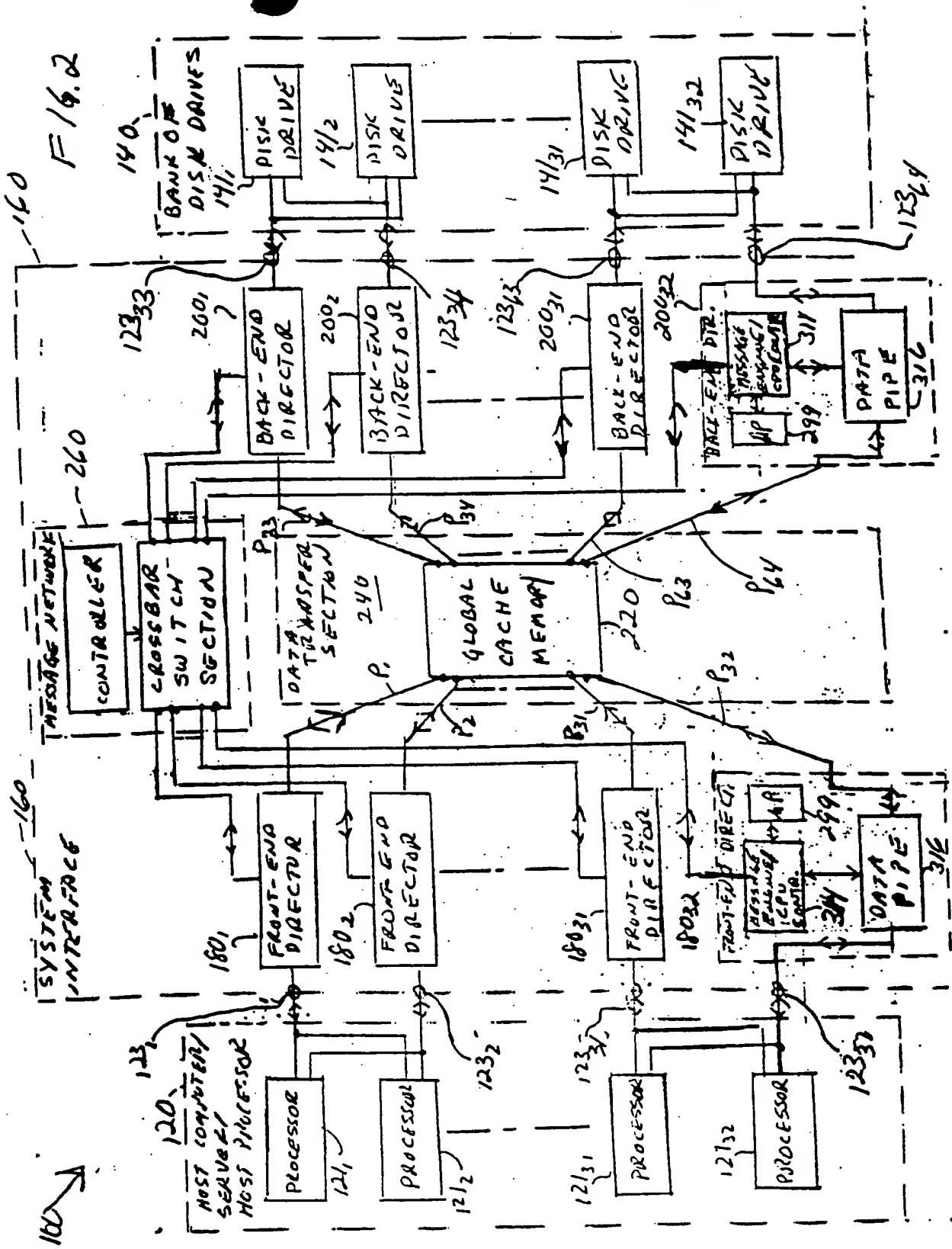


FIG. 3

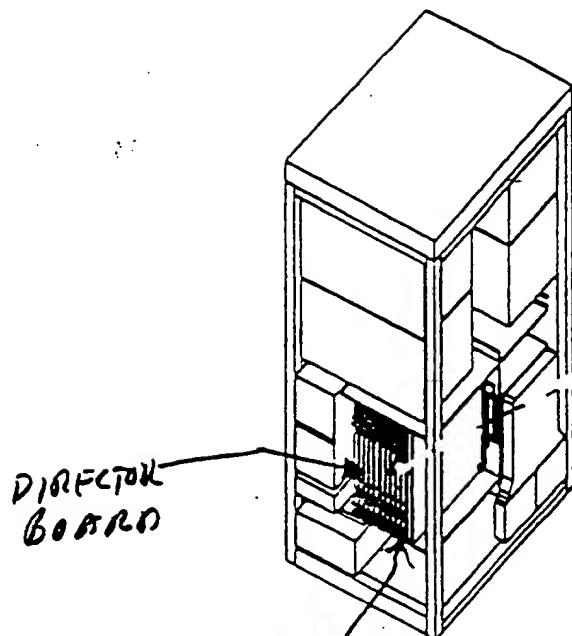


FIG. 4

CACHE MEMORY 220

BACK PLANE 302

MESSAGE NETWORK BOARD 30Y1

MESSAGE NETWORK BOARD 30Y2

TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER / SERVER / HOST PROCESSOR 120

DIRECTOR BOARD

DIRECTOR BOARD

DIRECTOR BOARD

DIRECTOR BOARD

DIRECTOR BOARD

DIRECTOR BOARD

BACK PLANE 302

CACHE MEMORY BOARD

CACHE MEMORY BOARD

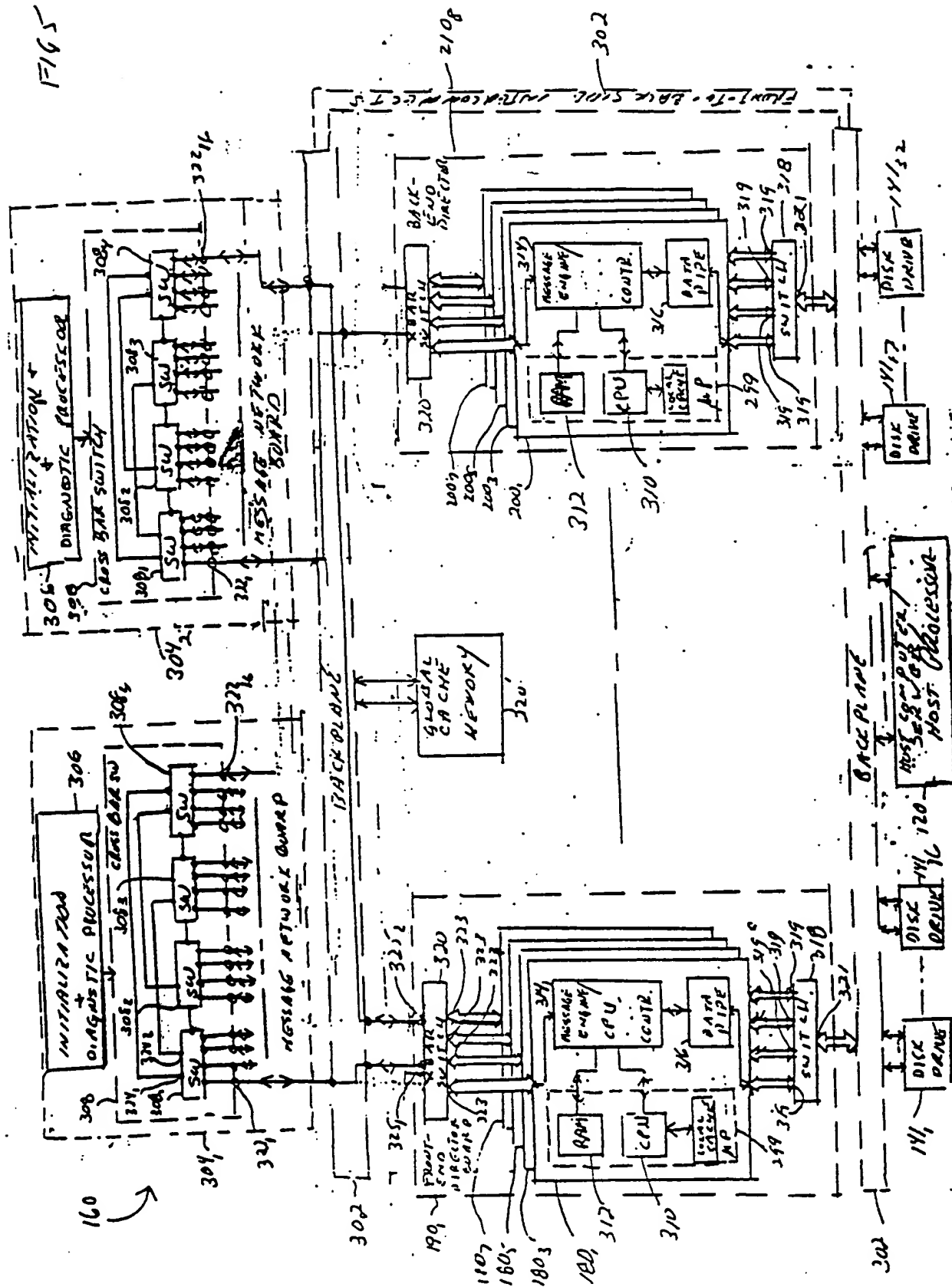


FIG. 7

DIRECTOR BOARD 1801

1801

TO/FROM
HOST
COMPUTER

PROTOCOL
TRANSLATOR

DATA
WIRE

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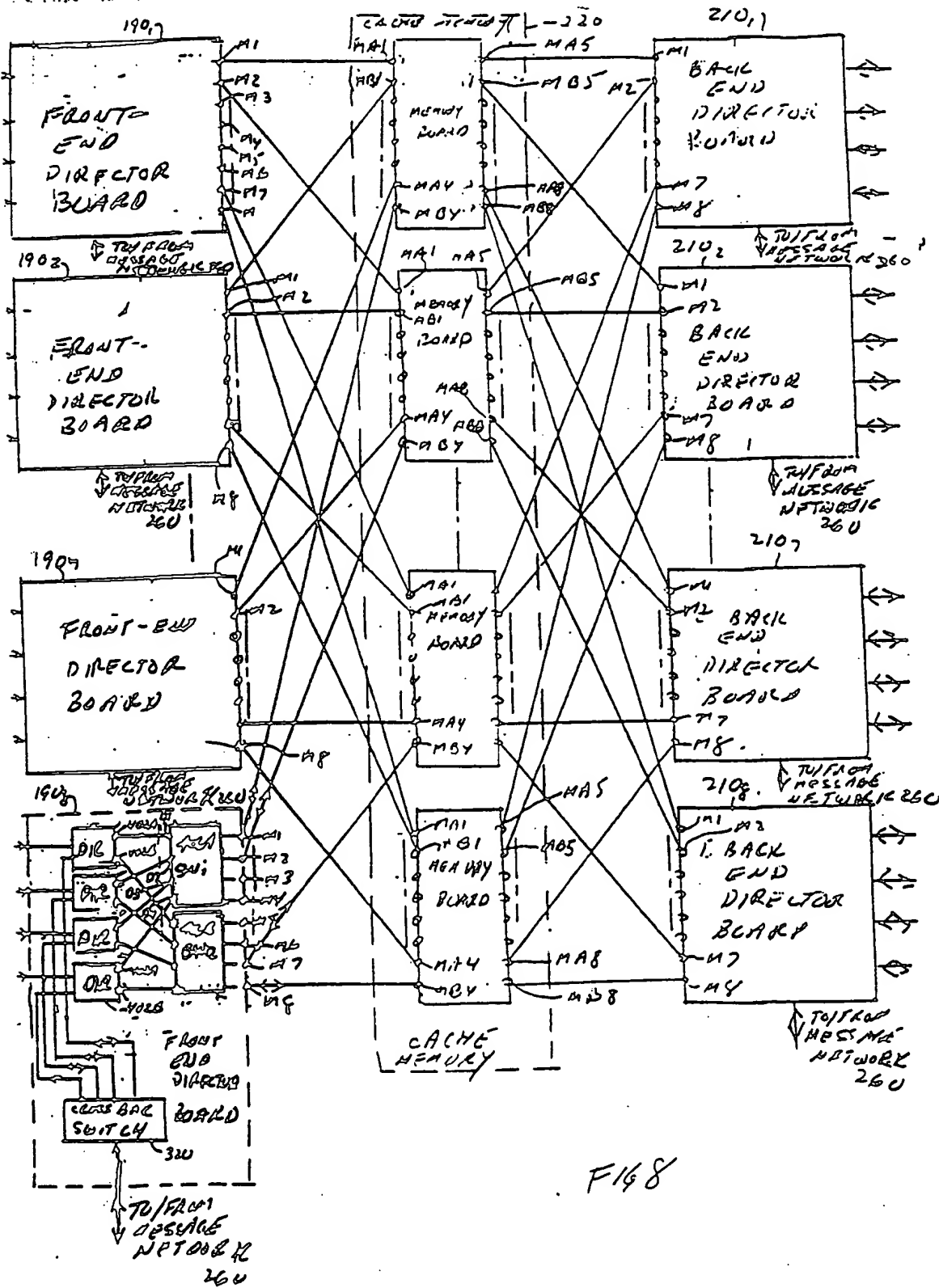


FIG 8

FIG 8A

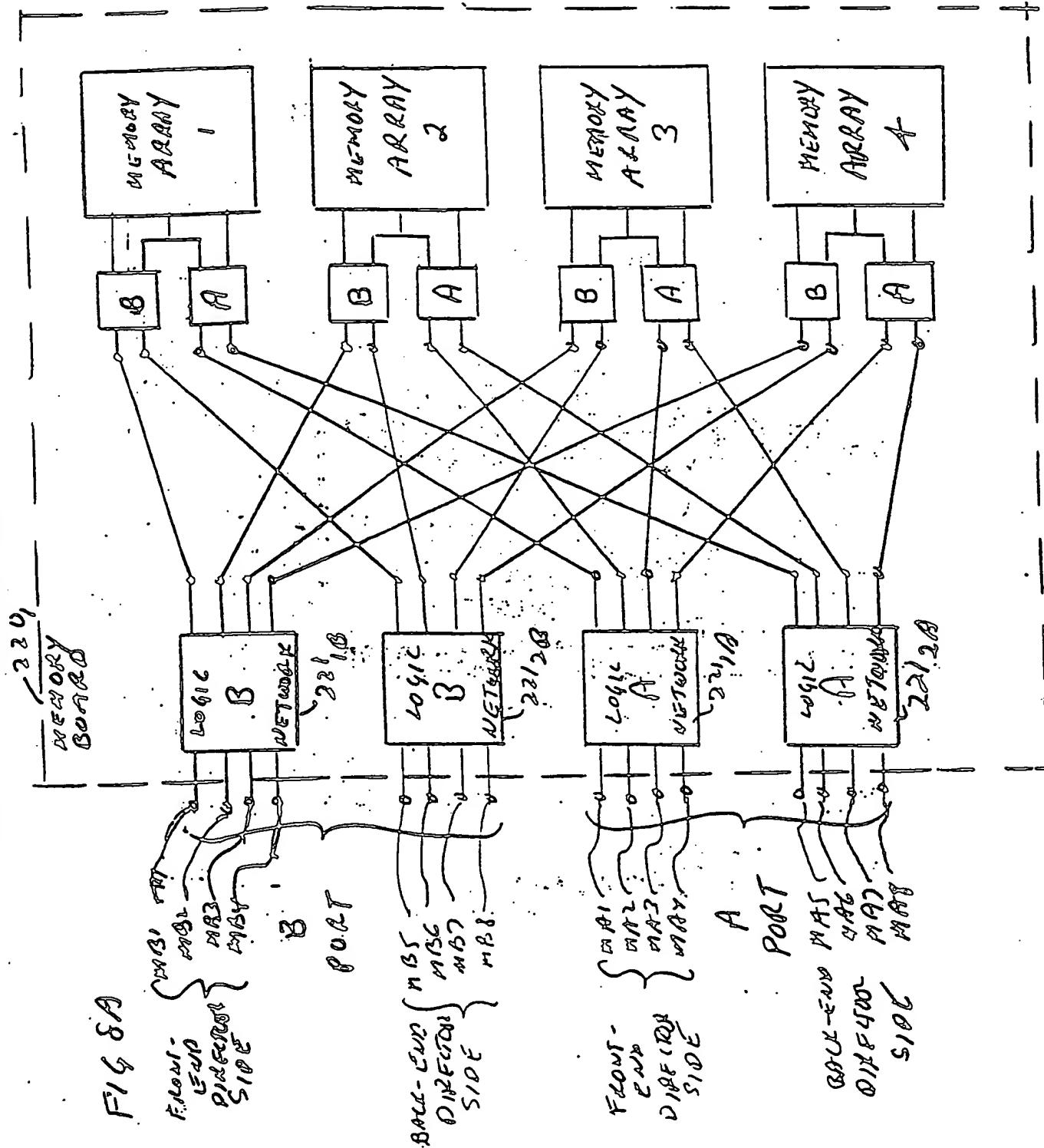


FIG 8B

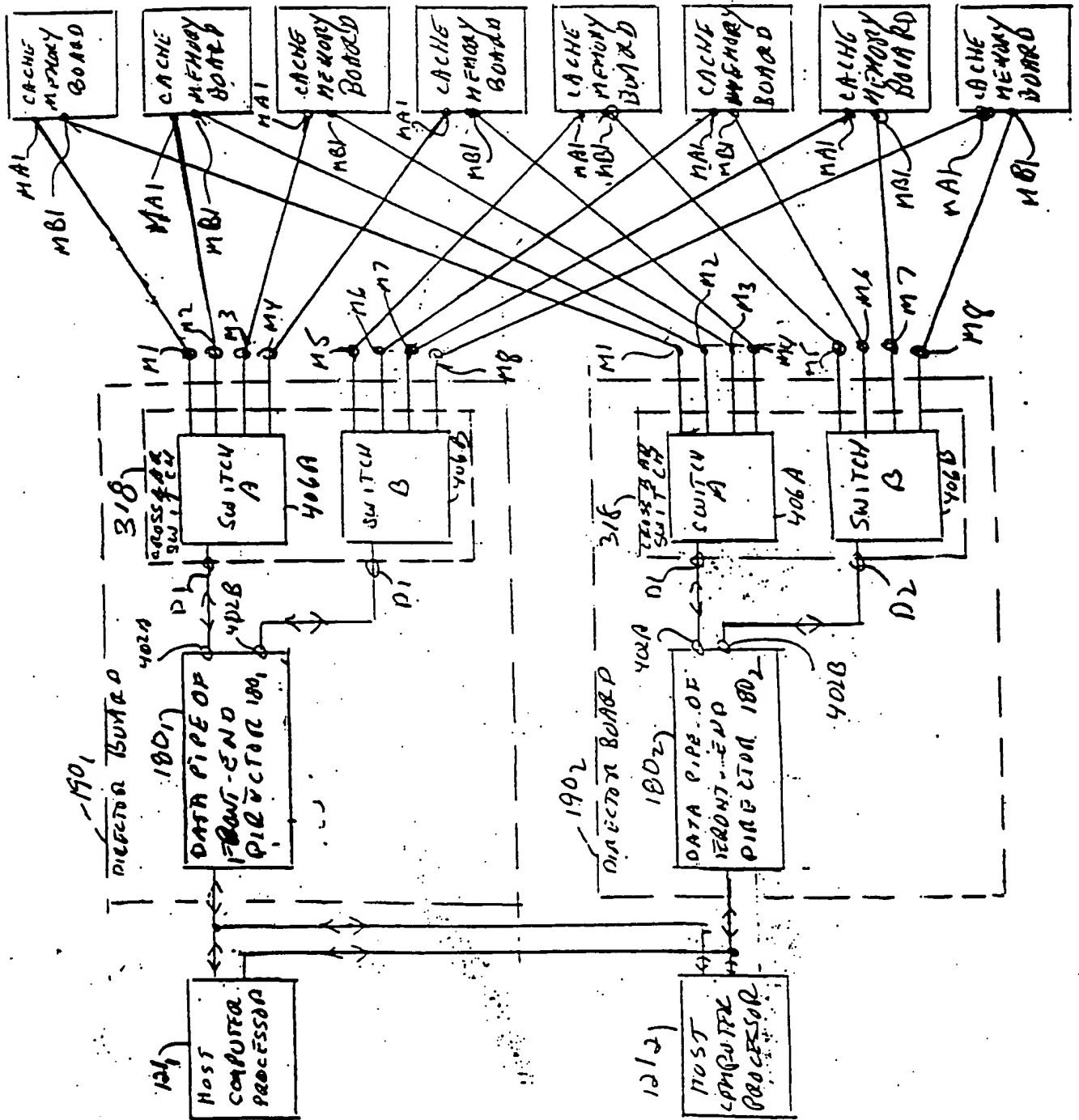
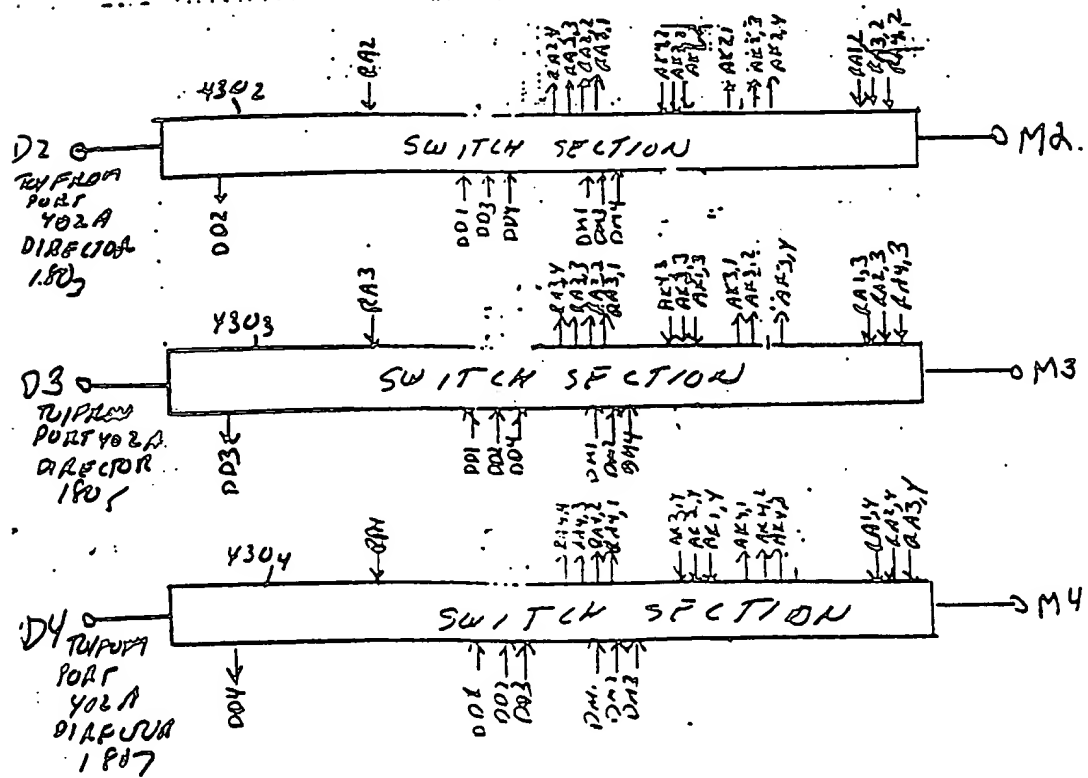
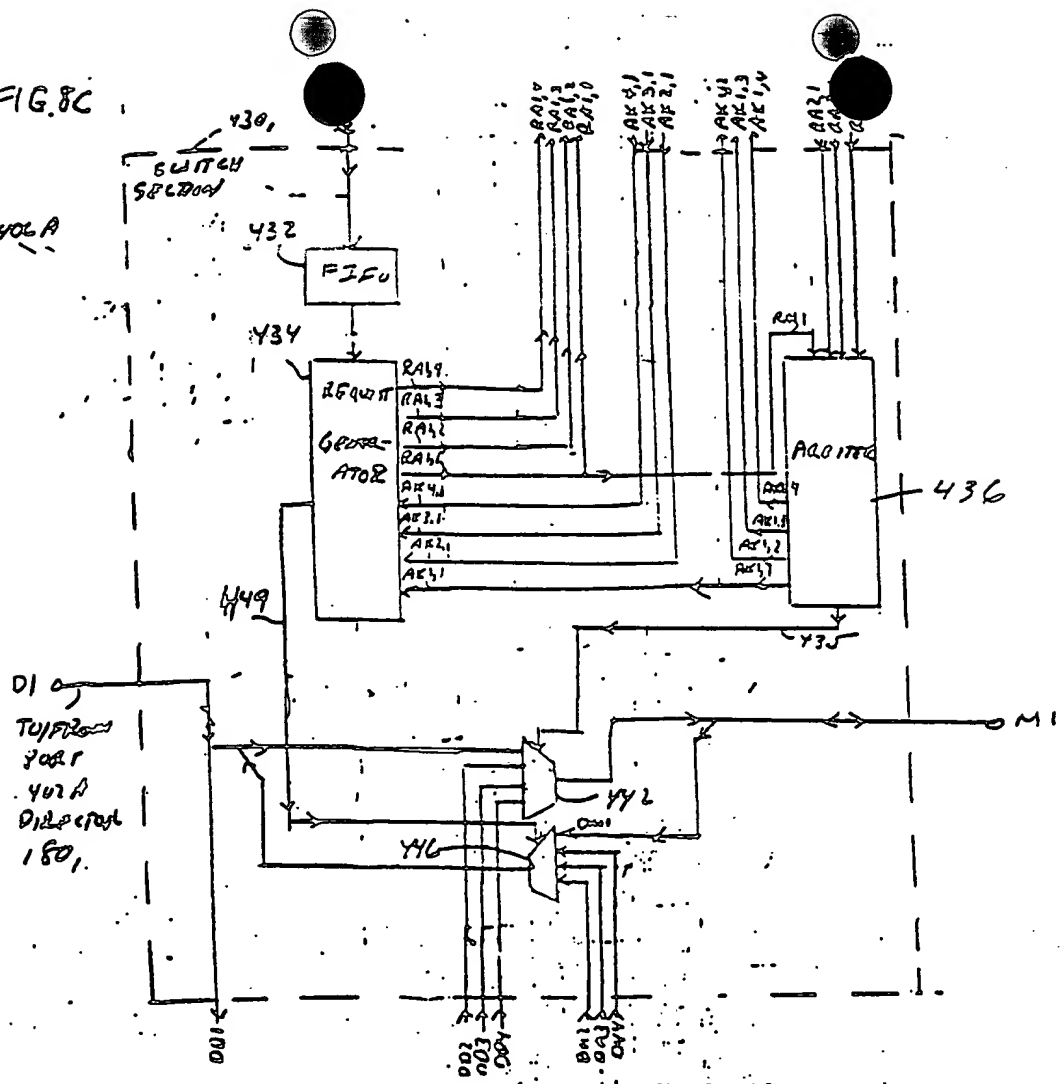
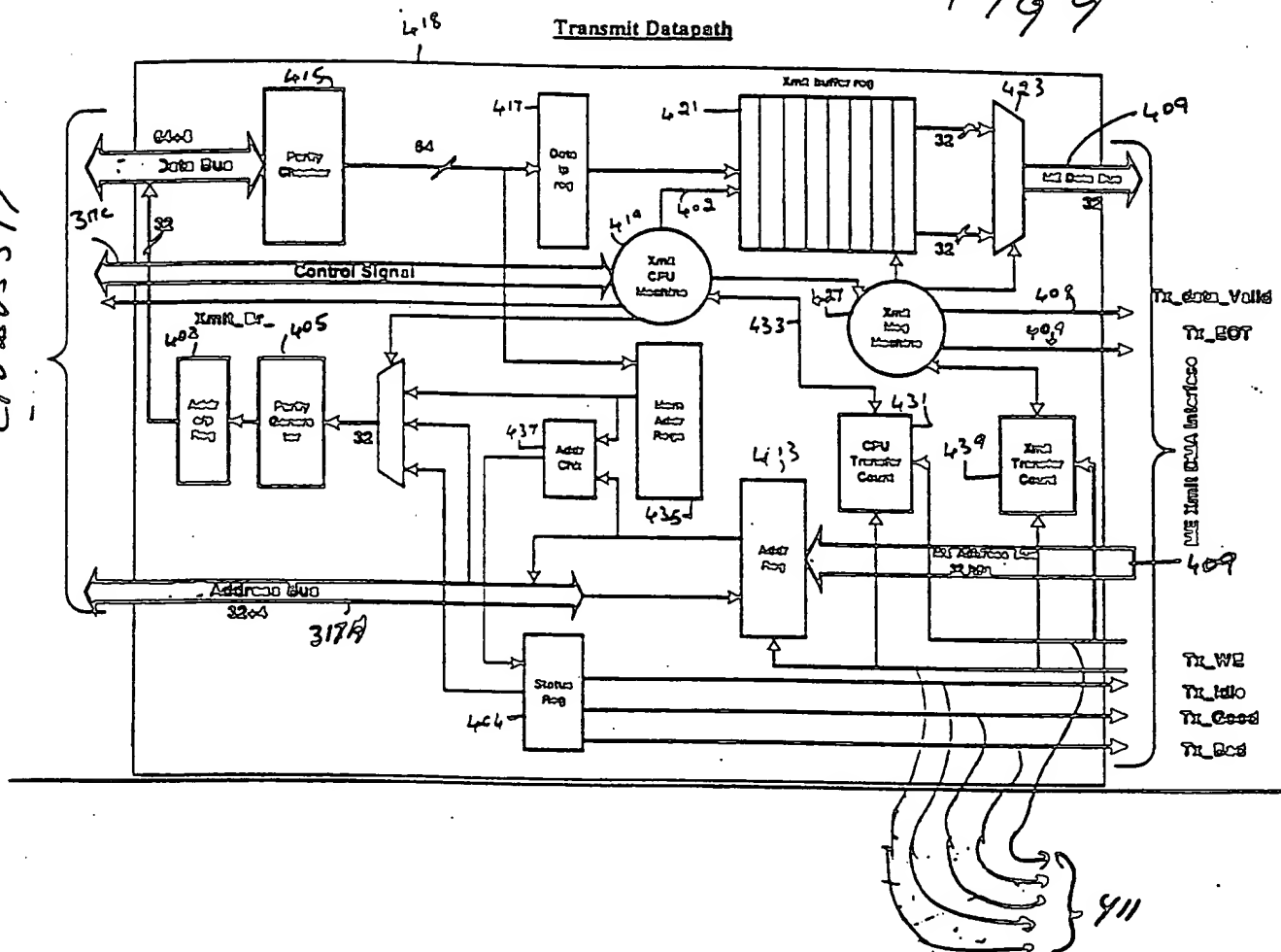


FIG. 8C

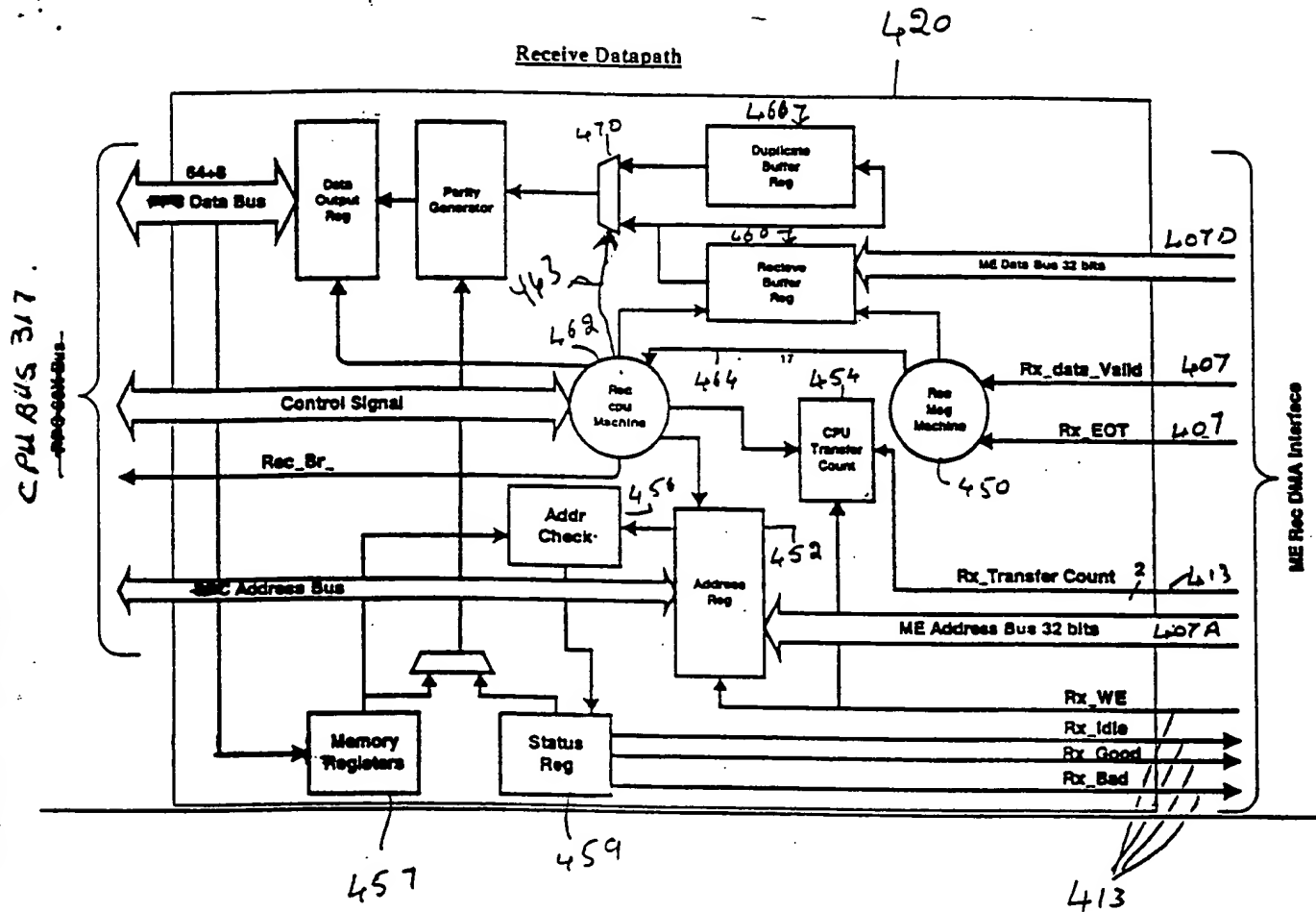
406A



CPU BUS 317



F1610



Message Bus Send Operation

FIG. 11A

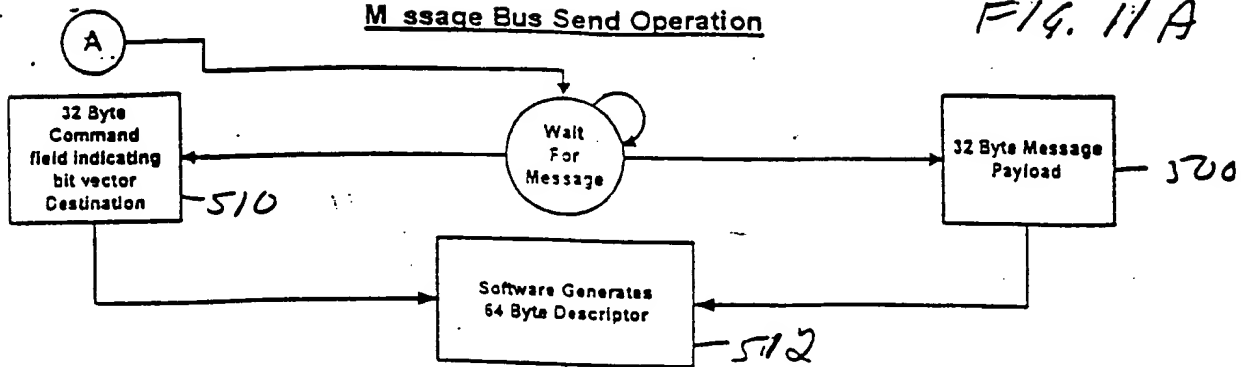


FIG 11

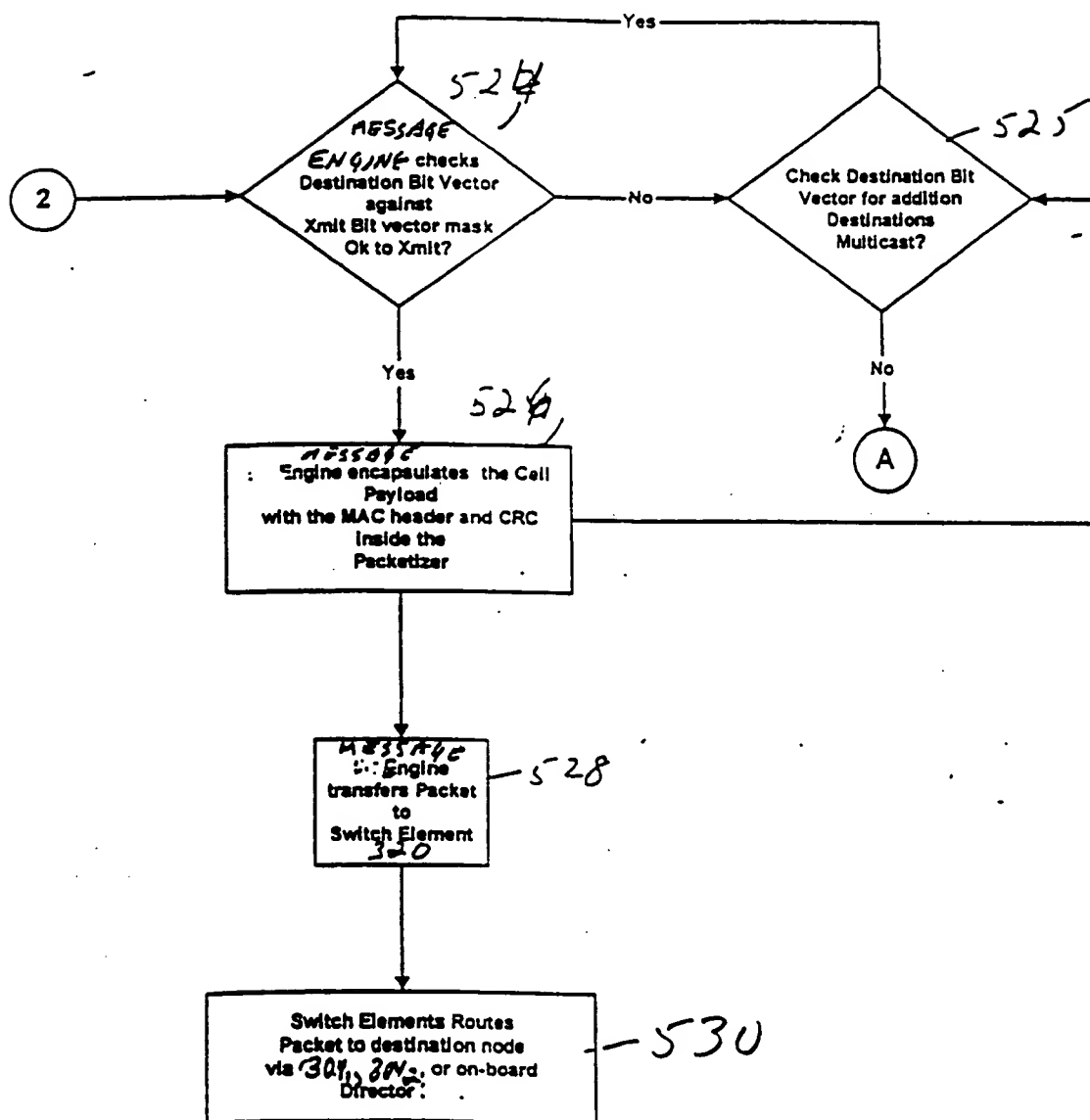
FIG 11A

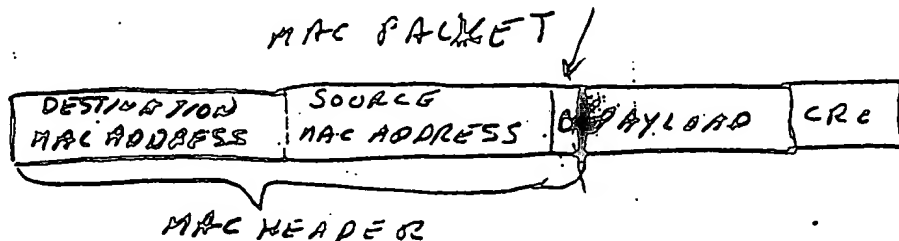
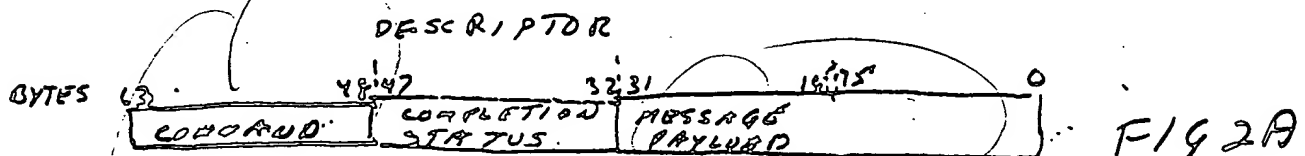
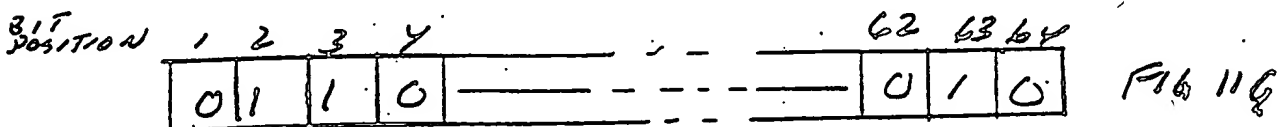
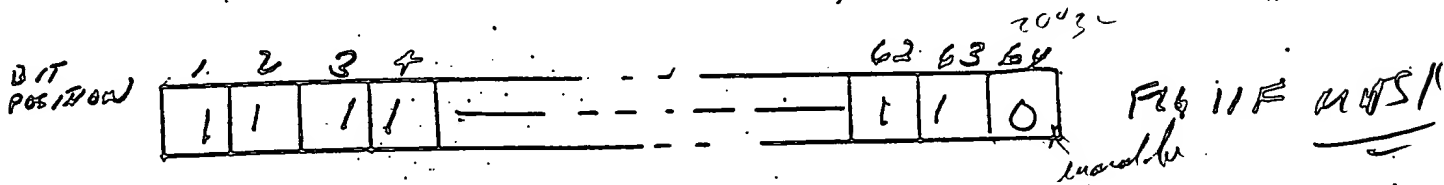
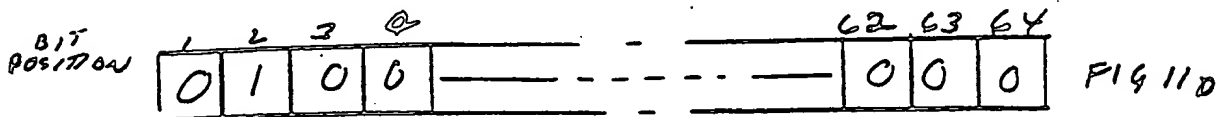
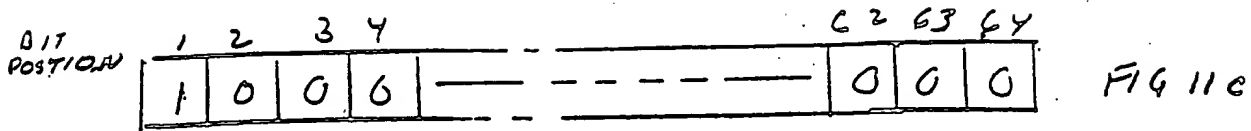
FIG 11B

2025-10-29 14:23:00

Message Bus Send Operation Continued

F1611B





Message Bus Receive Operation

FIG. 12A

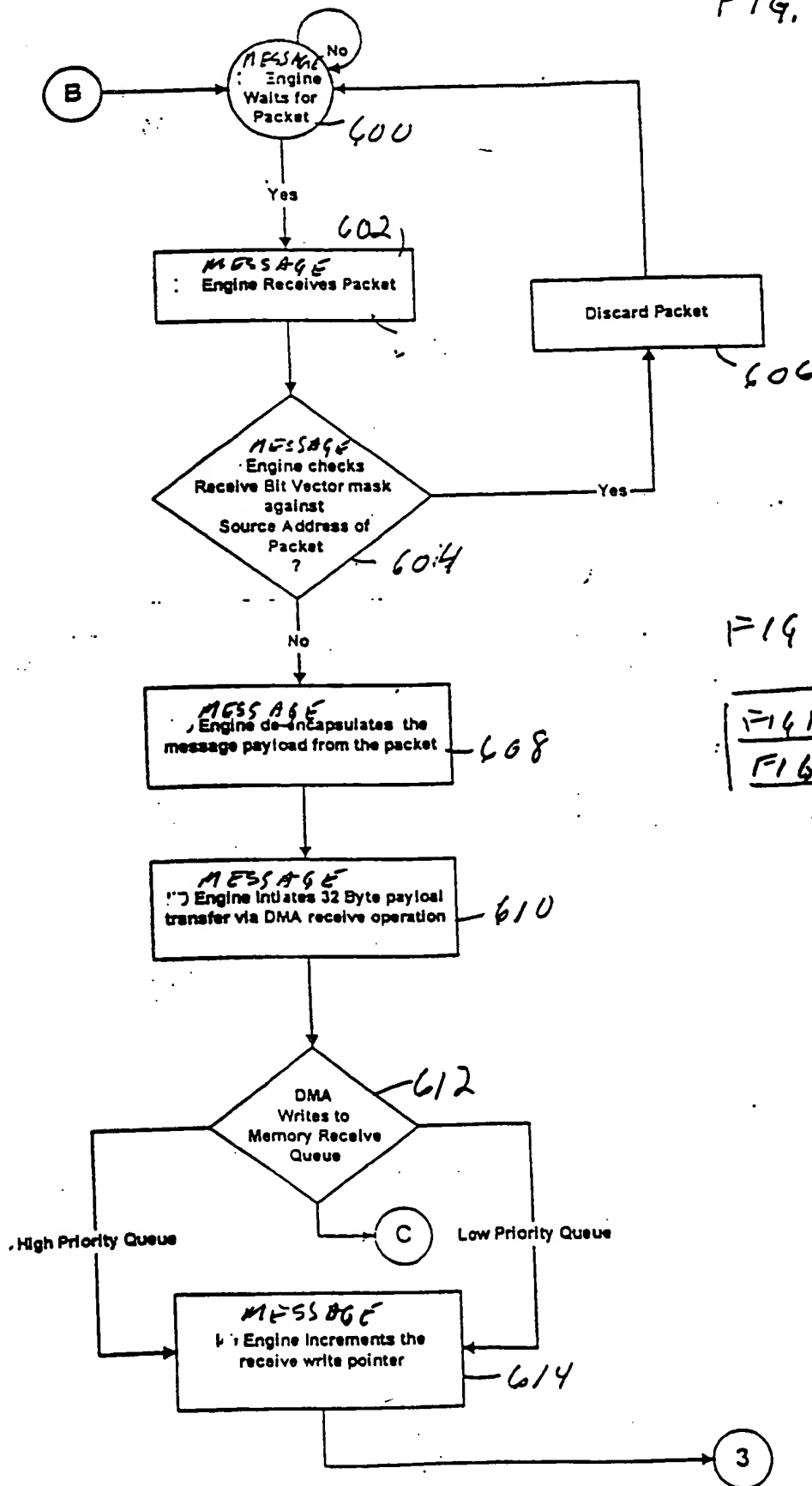
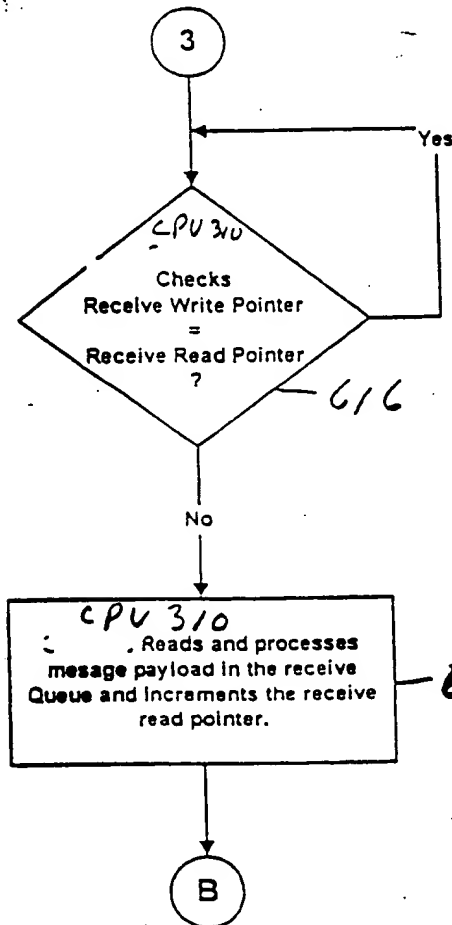


FIG 12

FIG 12A
FIG 12B

Message Bus Receive Operation Continued



F1412B

Message Bus Acknowledgement Operation

F-14.13

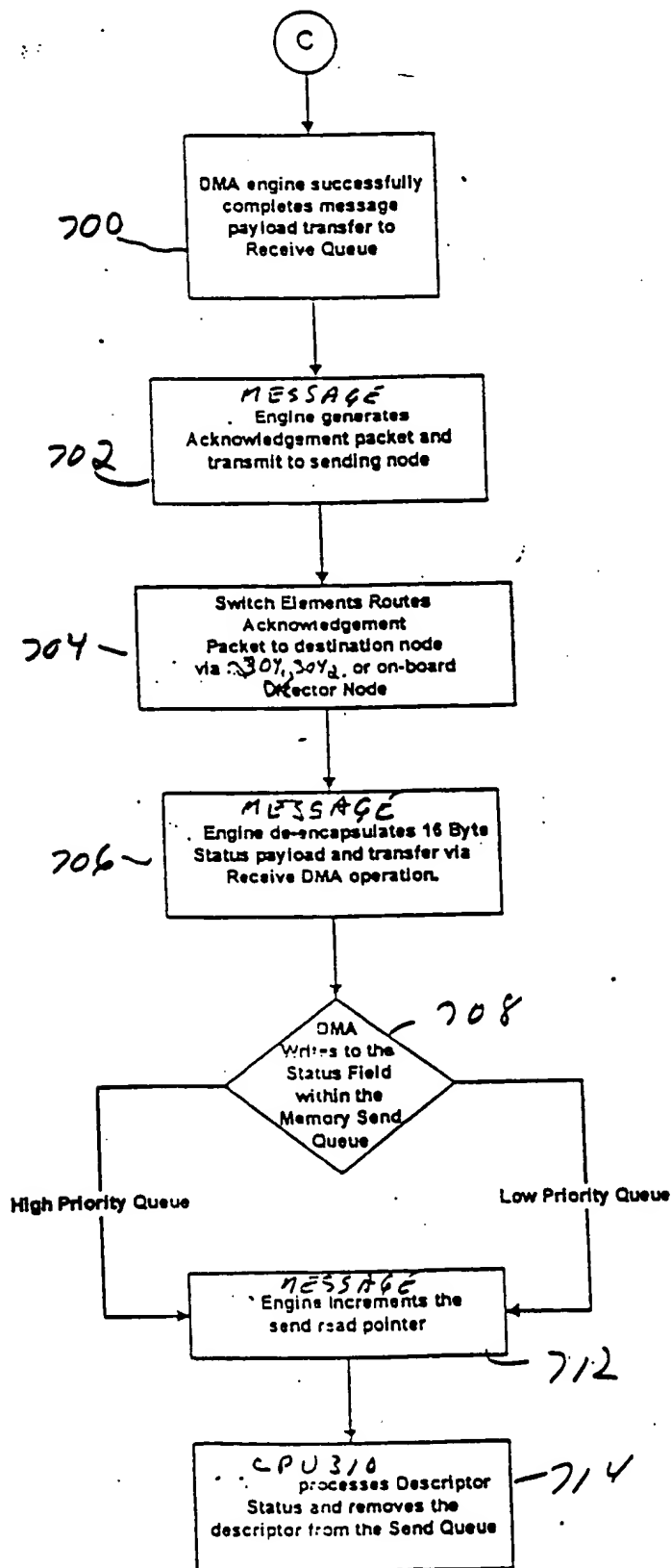
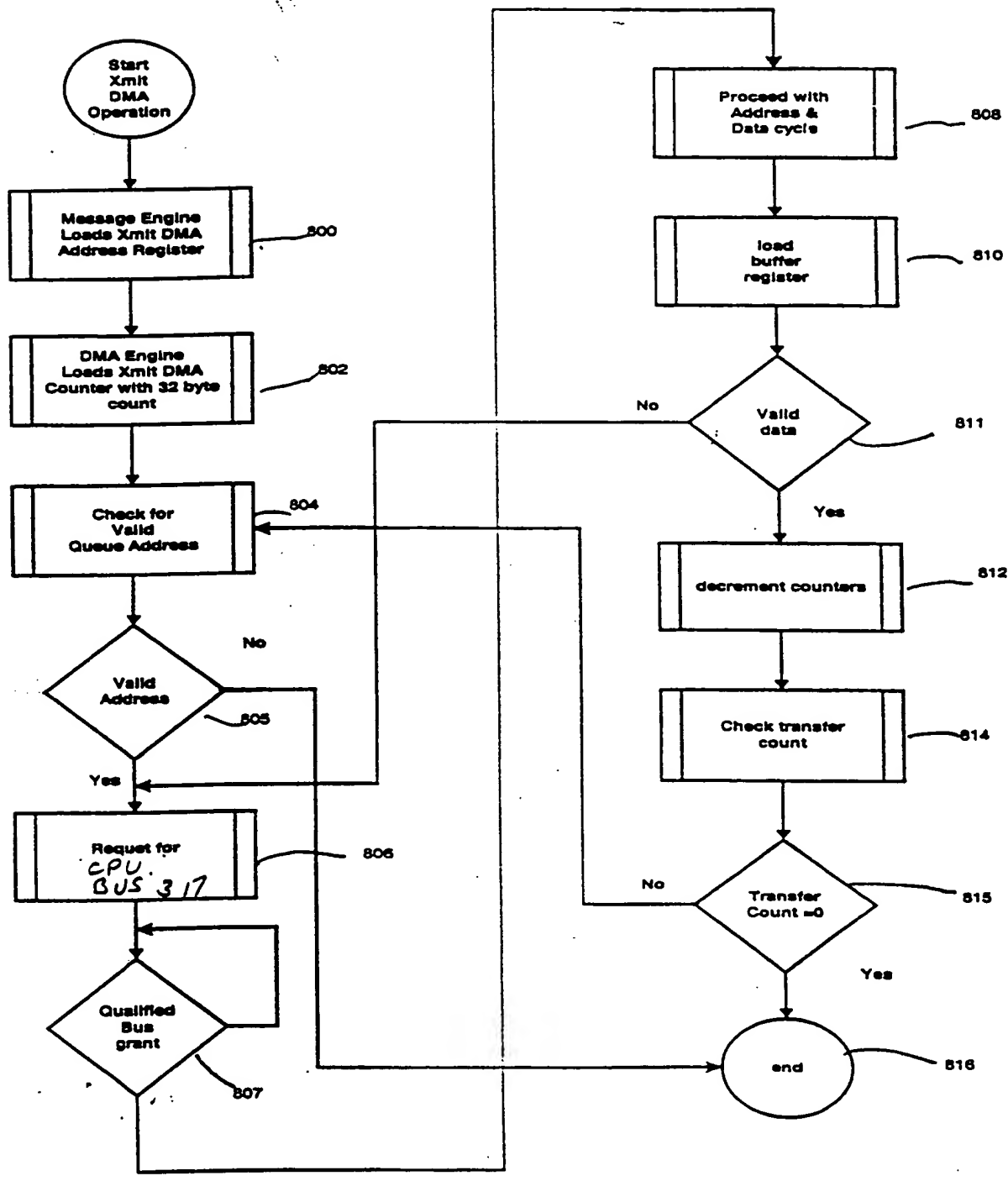


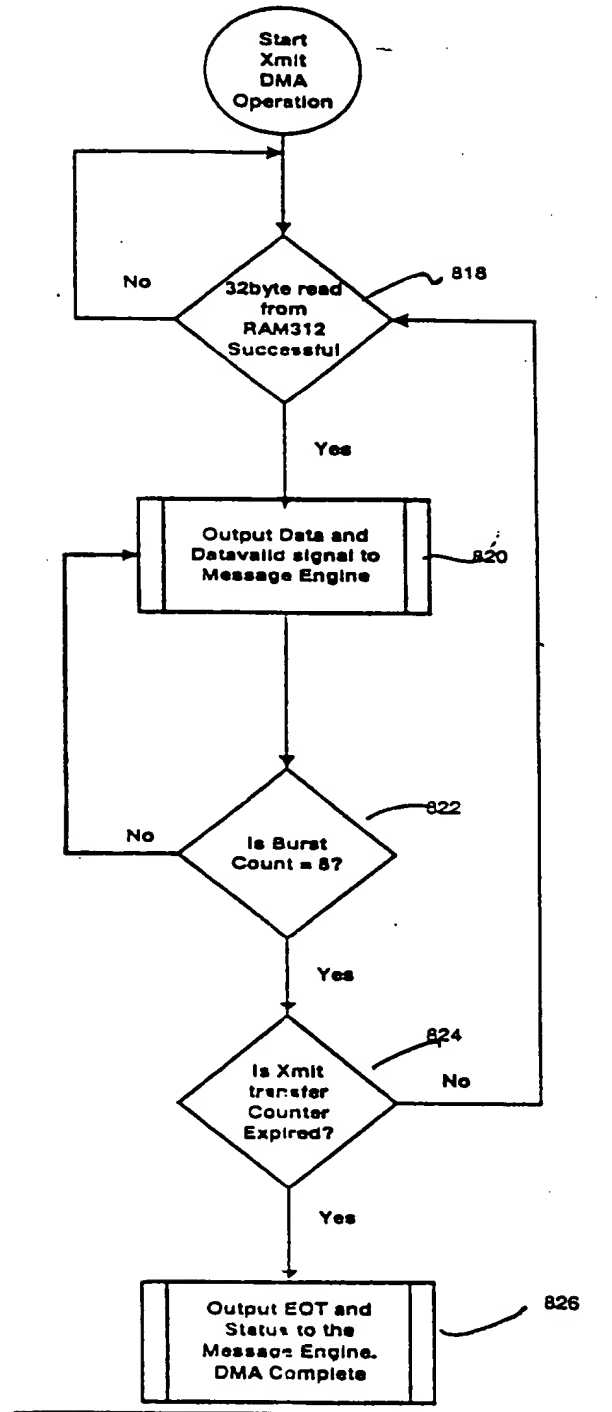
FIG 1A

Xmit CPU flow



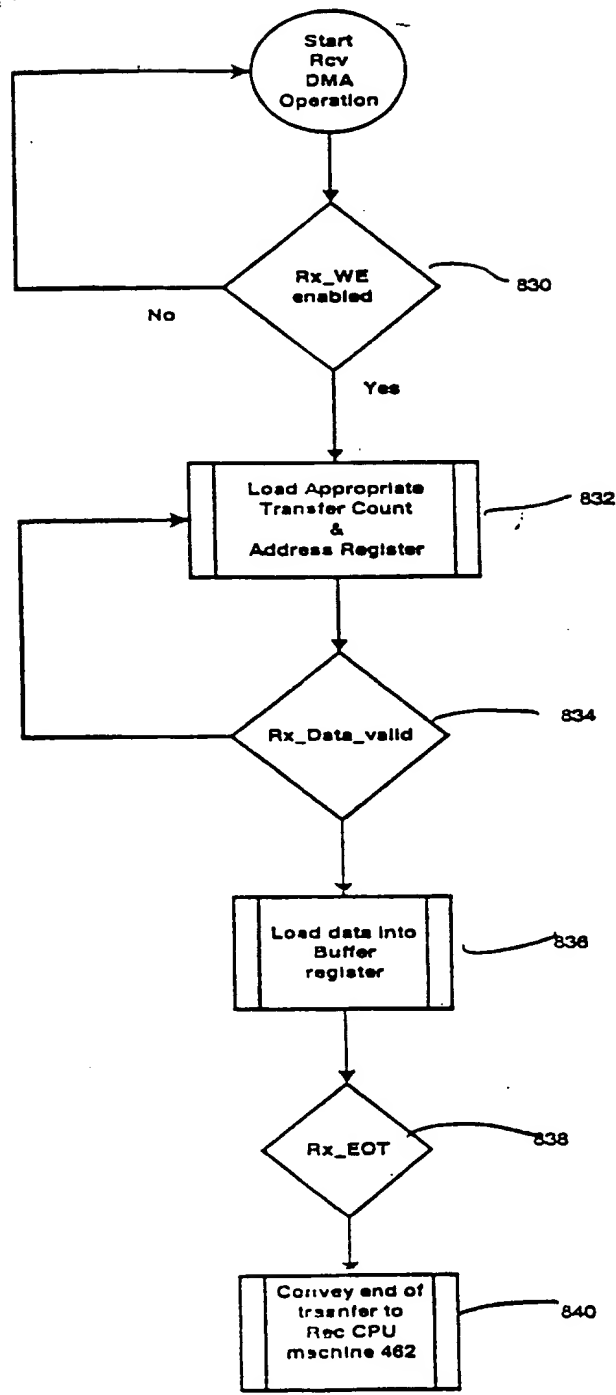
F1414B

Xmit Msg flow



F1615A

Rec msg fl w



P1415B

Rec cpu flow

